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(54) Process to create metallic stand-offs on a circuit board

(57) A process to create metallic stand-offs or studs on a printed circuit board (PCB). The process allows to obtain studs constituted by three successive layers of metal (Cu1, Cu2 and Cu3 or Ni) of which at least the two first layers are made of copper. The height of the so-create stand-off is sufficient to use it in the flip chip technology to assemble chips to a printed circuit board. The present process is implemented according either to the electro-plating (galvano-plating) or to the electrochemical-plating technique.

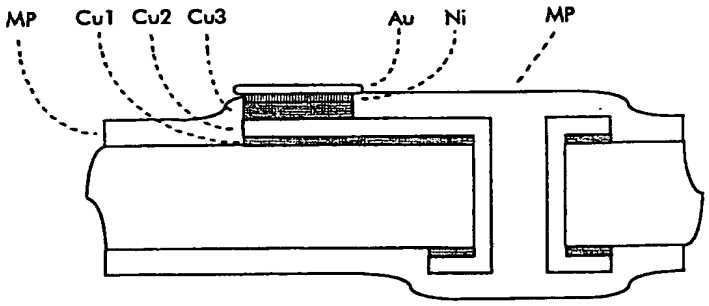

Fig. 10

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Descripti n

The present inv ntion relates to a process to create at least one stand-off on an electronic circuit.

Although not exclusively reserved therefore, this process is more particularly applicable to the known "flip chip" technology wherein several high density electronic chips are assembled onto a printed circuit board by means of so-called "stand-off's". A stand-off is a metallic stud or bump which, additionally to interconnecting the chip to the board, creates a distance between them. This distance is necessary to reduce fatigue effects in the interconnection due to differences in temperature expansion coefficients of the chip, generally constituted by silicon, and the carrier, i.e. the printed circuit board. The stud may obviously not collapse, especially during the assembly process.

Processes to create stand-offs or studs on a chip are already known in the art, e.g. from an IBM™ technology called "Controlled Collapsed Chip Connection" or "C4" technology. Therein, the studs are made using evaporation techniques through molybdenum masks. This known technology involves relatively expensive silicon back-end processing and, additionally, requires high cost mask material. A method for electrically connecting flip chips to a printed circuit substrate is for instance disclosed in the *US Patent No. 5,261,593* of Nov. 16, 1993, and an apparatus therefore is disclosed in the *US Patent No. 5,349,500* of Sep. 20, 1994.

In the known technologies, the stand-offs are realized on the chips, i.e. by the chip providers. Since several different chips are generally mounted on a same printed circuit board, the masks for the processing of these chips need to be created for relatively low production volumes. Furthermore, at least parts of these "bumping" processes are repeated by the different chip providers. All these elements lead to increase the production cost of the flip chip technology.

An object of the present invention is to reduce the number of operations of the chips and thereby to dramatically reduce the production cost of a flip chip assembly.

According to the invention, this object is achieved due to the fact that said stand-off is created on the surface of a printed circuit board constituting said electronic circuit and being coated with a first layer of copper, said process including the main successive steps of plating a second layer of copper at least onto predetermined portions of said first layer of copper, and of plating a third layer of metal on top of at least portions of said second layer of copper.

In this way, the stand-offs are constituted by three layers of metal located on top of each other on the surface of the printed circuit board, i.e., in case of the flip chip technology, on the surface of the carrier rather than on the surface of the chips. The assembly cost is reduced by the use f only one single back-end processing of the printed circuit board instead of dealing separately with several chips. In other words, the cost of the "bumping" process is reduced by staying independent of the different bumping technologies associated to different chips. Moreover, the fabrication of "non-melting" stand-offs, i.e. consisting of metals that are not melting during reflow soldering, gives a good control of the stand-off height between the chip and the printed circuit board after assembly.

In more detail, said process includes the steps of:

- depositing a first layer of photo-resistive material covering said first layer of copper;
- creating a first pattern uncovering said first layer of copper at least at the location of the future stand-off; and
- plating said second layer of copper onto the uncovered portion of said first layer of copper, said second layer of copper being substantially thicker than said first layer of copper.

Stand-offs constituted by two layers of copper are thereby created on the surface of the printed circuit board. However, for some applications the height of these stand-offs is not sufficient for create the above mentioned stand-off.

To this end, the process of the present invention can further be achieved by using either an electro-plating or an electrochemical-plating technique.

On the one hand, in case of using the electro-plating, also called galvano-plating, technique, the present process is further carried out by including the steps of:

- depositing a second layer of photo-resistive material;
- creating a second pattern uncovering said second layer of copper at least at the location of said future stand-off; and
- plating said third layer of metal onto the uncovered portion of said second layer of copper.

In this way, relatively high metallic stand-offs constituted by three successive layers of copper are created.

The present electro-plating process may be completed by further including the steps of:

- coating said third layer of metal with a protective layer of second metal;
- stripping said first and second layers of photo-resistive material;
- etching the unprotected layers of metal until the unprotected first layer of copper is removed; and
- stripping said protective layer of second metal.

Due to the relatively higher thickness of the second layer of copper with respect to that of the first layer of copper, the last etching step, which is a so-called differential etching step, removes the whole unprotected portions of the first layer of copper, while it only slightly

affect the thickness of the unprotected portions of th second layer of copper.

It is further to be noted that the metal of said third layer is preferably copper.

Finally, the present process may be completed by further including the step of electrochemical plating a layer of nickel onto the unprotected layers of copper, and the step of flash plating a layer of gold onto said layer of nickel.

On the other hand, in case of using the electrochemical-plating technique, the above process of the present invention is further carried out by including the steps of:

- coating said second layer of copper with a protective layer of second metal;
- stripping said first layer of photo-resistive material;
- etching the unprotected first layer of copper;
- stripping said protective layer of second metal,
- depositing a layer of photo sensitive dielectric material;
- creating a second pattern removing said layer of photo sensitive dielectric material at the location of said future metallic stand-off; and
- plating a third layer of metal onto the uncovered portions of said second layer of copper.

In this way, a relatively high metallic stand-off constituted by three successive layers of metal is created.

In a first embodiment of the present electrochemical-plating process, the metal of said third layer is copper.

The process then further includes the steps of electrochemical plating a layer of nickel onto said stand-off using said layer of photo sensitive dielectric material as mask.

In a second embodiment of the present electrochemical-plating process, the metal of said third layer is nickel.

The electrochemical-plating process is then completed by further including the step of flash plating a layer of gold onto said layer of nickel using said layer of photo sensitive dielectric material as mask.

A good electric contact terminal or pad is thereby realized.

In the above processes, the second metal of said protective layer is preferably tin-lead.

The present technology can be applied to very large area substrates, i.e. different dimensions of printed circuit boards, combining several different flip chip Input/Output (I/O) locations in one design and manufacturing process. It further can accommodate the assembly of most standard available chips.

The above mentioned and other objects and features of the invention will become more apparent and the invention itself will be best understood by referring to the following description of an embodiment taken in conjunction with the accompanying drawings wh rein:

Fig's. 1 to 3 show common steps for the electro-plating and the electrochemical-plating process according to the invention;

Fig's. 4 to 6 show further steps of the electro-plating process; and

Fig's. 7 to 10 show further steps of the electrochemical-plating process.

The process show in the drawings Fig's 1 to 10 is used to create metallic bumps or stand-offs on the surface of a printed circuit board in order to realize a flip chip assembly.

The drawings show a portion of a transversal section of a printed circuit board PCB provided with a hole. The board PCB is coated on its upper and lower surface with a basis layer of copper Cu1 as shown in Fig. 1. The processing steps described below lead to obtain, on the board PCB, an optimal combination of conductive copper paths, elevated stand-offs and plated-through holes, the stand-offs being used to allow external Input/Output (I/O) connections to flip chips and are also called "studs".

In the following part of the description, two possible techniques used to create a metallic stand-off and a plated-through hole will be explained. The successive processing steps according to a first technique, called electro- or galvano-plating technique, are represented in the Fig's 1 to 6, whilst the successive processing steps according to a second technique, called electrochemical-plating technique, are represented in the Fig's 1 to 3 and 7 to 10. The Fig's 1 to 3 are thus common for these two techniques and will be explained only once below.

The first step of the present process consists in depositing a first layer of photo-resistive material PR1 covering the basis layer of copper Cu1 on both sides of the PCB. A pattern is then created in the photo-resistive material PR1 according to a technique well known in the art and therefore not explained in more detail hereafter. Fig. 2 shows the board after the creation of the pattern on the layer PR1.

A further step of the process consists in plating a second layer of copper Cu2 onto the uncovered portions of the basis or first layer of copper Cu1, i.e. by using the patterned layer PR1 as mask. The second layer of copper Cu2 has a thickness which is substantially larger than that of the first layer of copper Cu1. This second layer of copper Cu2 is not only deposited onto the uncovered portions of Cu1 but also in the hole drilled through the printed circuit board PCB as shown in Fig. 3.

The above mentioned two techniques differentiate now. The following explanations relate to the electro-plating or galvano-plating technique, and the electrochemical-plating technique will be explained later starting from this step.

In the electro-plating technique, the next step consists in depositing a second layer of photo-resistive

material PR2 on the device as shown in Fig. 3. A pattern is then create on the second photo-resistive layer PR2 leaving uncovered the portions of copper Cu2 at the location of the future stand-off. A further step of this process consists in plating a third layer of copper Cu3 on these uncovered portions of Cu2. Still by using the second patterned layer PR2 as mask, a protective metallic layer of tin-lead SnPb is deposited on top of the layer Cu3. The result is shown in Fig. 4.

The two layers PR1 and PR2 of photo-resistive material are then stripped away. Afterwards, the unprotected portions of the layers of copper Cu1 and Cu3 are etched until the uncovered portions of the layer Cu1 are removed from the board PCB as shown in Fig. 5.

After this differential etching of the copper layers Cu1 and Cu2 using the tin-lead layer SnPb as mask, the remaining overall thickness of the two layers of copper Cu1 and Cu2 is of about 35 µm.

Finally the protective metallic layer of tin-lead SnPb is stripped away and a high stand-off comprising the three successive layers of copper Cu1, Cu2 and Cu3 is created as shown in Fig. 6. The height of the metallic stand-off is between 50 and 75 µm.

The still unprotected layers of copper Cu2 and Cu3 may then be coated by a relatively thin protective layer of nickel electrochemically plated thereon. A good electric contact may further be achieved by flash plating a layer of gold on top of the protective layer of nickel. The result of these last plating steps are not shown in the figures.

This completes the electro-plating technique.

In the electrochemical-plating technique, the step following the one shown in Fig. 3 is represented in Fig. 7 and consists in depositing a protective metallic layer of tin-lead SnPb on top of the layer Cu2, using the patterned photo-resistive layer PR1 as mask. The protective layer SnPb is deposited in a galvanic way as known in the art.

The photo-resistive layer PR1 is then stripped away and the remaining uncovered portions of the basis layer of copper Cu1 are etched using the layer SnPb as a mask. The result is shown in Fig. 8.

The following step consists in stripping the protective metallic layer SnPb. A layer of photo sensitive dielectric material MP is then deposited over the whole device as shown in Fig. 9. Such a deposition may for instance be realized by means of the known "curtain coating" technique and the dielectric layer MP is for instance constituted by the so-called "multiposit™ material of the company "Shipley". The reason of depositing a layer of photo sensitive dielectric material MP rather than a photo-resistive layer is that the latter does not resist to a nickel-gold deposition as will be performed later.

A pattern is then created in the dielectric layer MP as shown in Fig. 9. This pattern defines the position of the stand-off in a photo-lithographic way by removing the layer of photo sensitive dielectric material MP at the location of this future stand-off.

According to a first variant of realization, a third layer of copper Cu3 is plated onto the then uncovered portions of the second layer of copper Cu2. A high stand-off comprising the three successive layers of copper Cu1, Cu2 and Cu3 is so created.

As for the above described galvano-plating technique, the third layer of copper Cu3 may then be coated by a relatively thin protective layer of nickel Ni electrochemically plated thereon. This plating process uses the dielectric layer MP as a mask. The process is completed with a flash deposition or plating of gold Au over the nickel layer Ni. Here again the dielectric layer MP is used as a mask. The thickness of the gold layer Au is of about 0.1 µm and is used to improve the electric contact with the chip to be connected to the stand-off.

According to another variant of realization, not shown in the figures, a relatively thick layer of nickel is plated onto the uncovered portions of the second layer of copper Cu2. The so-created stand-off is then constituted by two layers of copper Cu1 and Cu2 and a thick layer of nickel. Here again the layer of nickel may be covered by a layer of gold to provide a good electric contact. It is to be noted that the layers of nickel and gold are deposited by using the dielectric layer MP as a mask and that the gold layer is preferably deposited according to the flash plating technique.

While the principles of the invention have been described above in connection with specific apparatus, it is to be clearly understood that this description is made only by way of example and not as a limitation on the scope of the invention.

Claims

1. Process to create at least one stand-off on an electronic circuit, characterized in that said stand-off is created on the surface of a printed circuit board (PCB) constituting said electronic circuit and being coated with a first layer of copper (Cu1), said process including the main successive steps of plating a second layer of copper (Cu2) at least onto predetermined portions of said first layer of copper (Cu1), and of plating a third layer of metal (Cu3, Ni) on top of at least portions of said second layer of copper (Cu2).

2. Process according to claim 1, characterized in that said process includes the steps of:

   - depositing a first layer of photo-resistive material (PR1) covering said first layer of copper (Cu1);
   - creating a first pattern uncovering said first layer of copper (Cu1) at least at the location of the future stand-off; and
   - plating said second layer of copper (Cu2) onto the uncov red porti n of said first layer of cop-

per (Cu1), said second layer of copp r (Cu2) being substantially thicker than said first layer of copper (Cu1).

3. Process according to claim 2, characterized in that said process further includes the steps of:

   - depositing a second layer of photo-resistive material (PR2);
   - creating a second pattern uncovering said second layer of copper (Cu2) at least at the location of said future stand-off; and
   - plating said third layer of metal (Cu3) onto the uncovered portion of said second layer of copper (Cu2).

4. Process according to claim 3, characterized in that said process further includes the steps of:

   - coating said third layer of metal (Cu3) with a protective layer of second metal (SnPb);
   - stripping said first (PR1) and second (PR2) layers of photo-resistive material;
   - etching the unprotected layers of metal until the unprotected first layer of copper (Cu1) is removed; and
   - stripping said protective layer of second metal (SnPb).

5. Process according to claim 4, characterized in that the metal of said third layer is copper (Cu3).

6. Process according to claim 5, characterized in that it further includes the step of electrochemical plating a layer of nickel onto the unprotected layers of copper (Cu2, Cu3).

7. Process according to claim 6, characterized in that it further includes the step of flash plating a layer of gold onto said layer of nickel.

8. Process according to claim 2, characterized in that said process further includes the steps of:

   - coating said second layer of copper (Cu2) with a protective layer of second metal (SnPb);
   - stripping said first layer (PR1) of photo-resistive material;
   - etching the unprotected first layer of copper (Cu1);
   - stripping said protective layer of second metal (SnPb),
   - depositing a layer of photo sensitive dielectric material (MP);
   - creating a second pattern removing said layer of photo sensitive dielectric material (MP) at the location of said future metallic stand-off; and
   - plating said third lay r of metal (Cu3, Ni) onto the uncovered portion of said second layer of copper (Cu2).

9. Process according to claim 8, characterized in that the metal of said third layer is copper (Cu3).

10. Process according to claim 9, characterized in that it further includes the step of electrochemical plating a layer of nickel (Ni) onto said stand-off using said layer of photo sensitive dielectric material (MP) as mask.

11. Process according to claim 8, characterized in that the metal of said third layer is nickel (Ni).

12. Process according to any of the claims 10 or 11, characterized in that it further includes the step of flash plating a layer of gold (Au) onto said layer of nickel (Ni) using said layer of photo sensitive dielectric material (MP) as mask.

13. Process according to any of the claims 4 or 8, characterized in that the second metal of said protective layer (SnPb) is tin-lead.

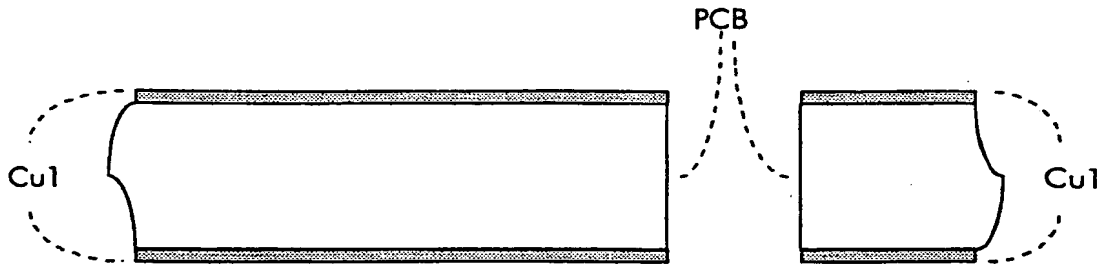

Fig. 1

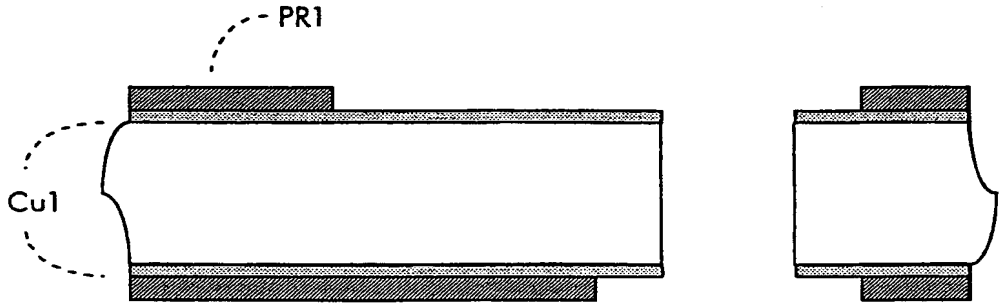

Fig. 2

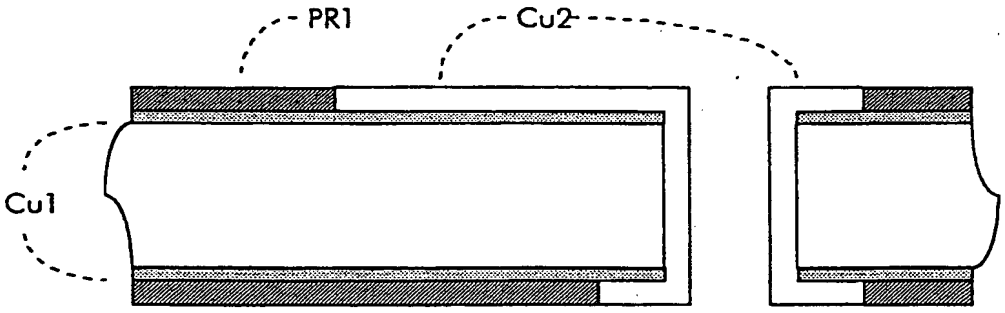

Fig. 3

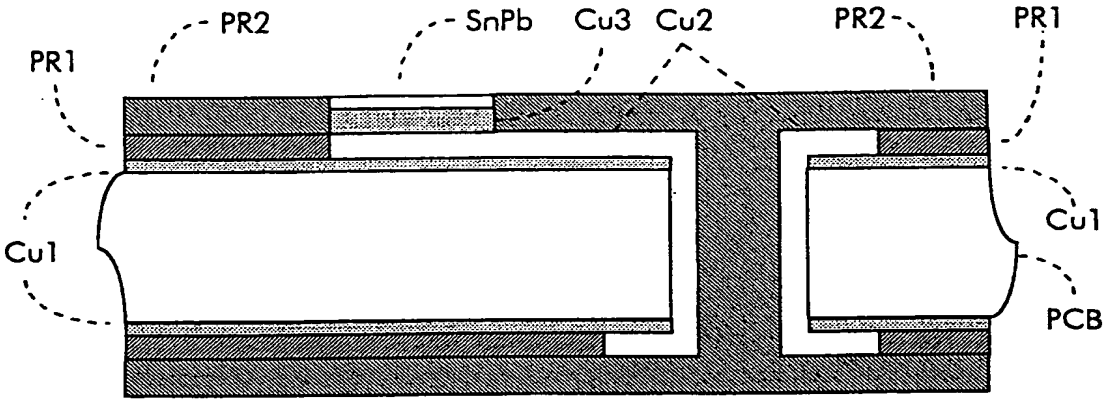

Fig. 4

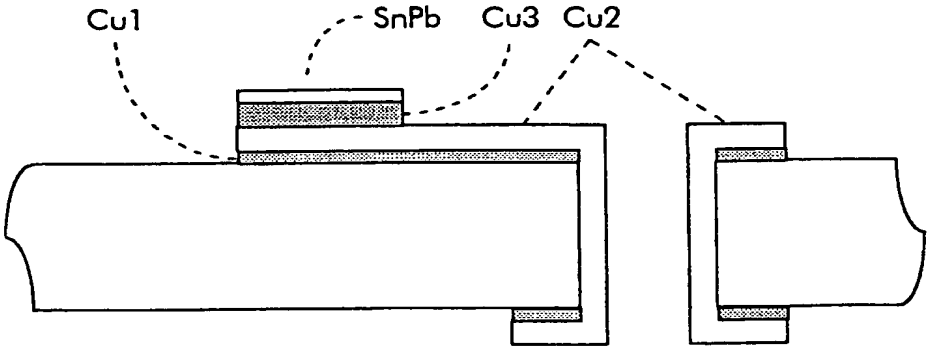

Fig. 5

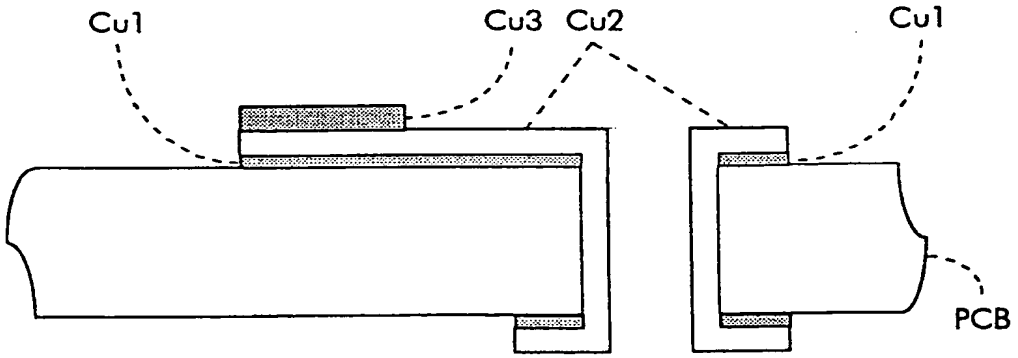

Fig. 6

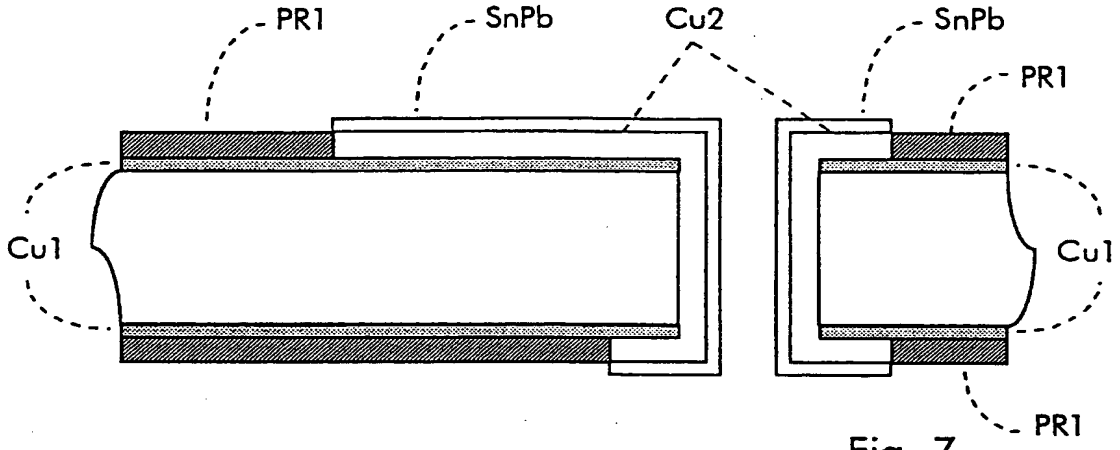

Fig. 7

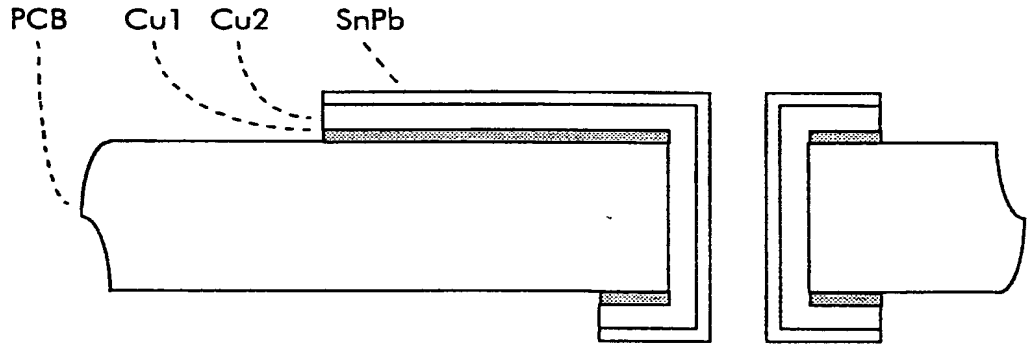

Fig. 8

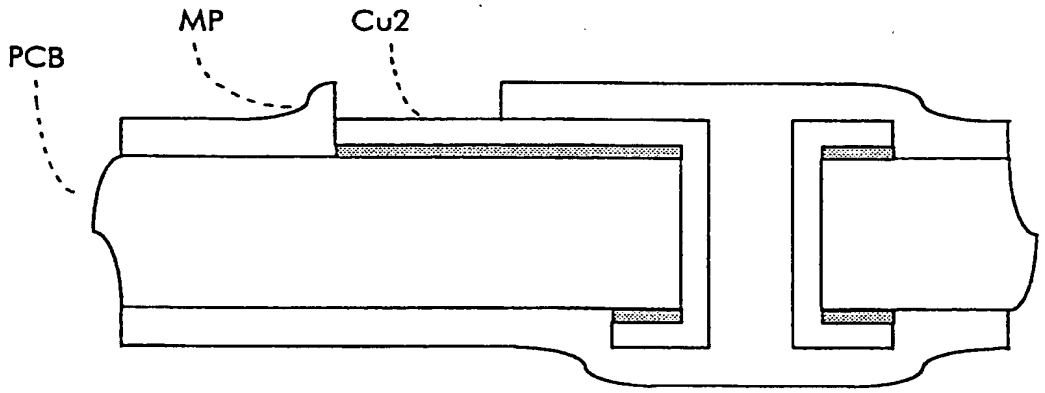

Fig. 9

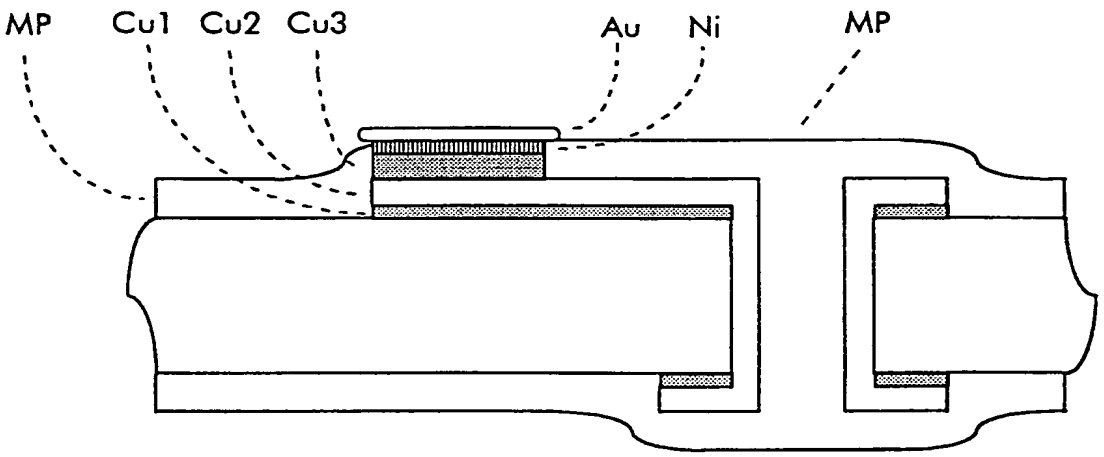

Fig. 10

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Application Number
EP 96 40 2845

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X Y	US 5 283 948 A (SCHROEDER PAUL E ET AL) 8 February 1994 * the whole document *	1-5 6-13	H05K3/40 H05K3/24 H01L21/48 H01L23/492
Y	US 5 118 386 A (KATAOKA TATSUO ET AL) 2 June 1992 * the whole document *	6-13	
A	WO 95 05675 A (EPOXY TECHNOLOGY INC) 23 February 1995 * the whole document *	1-13	
A	EP 0 354 671 A (UNIV CALIFORNIA) 14 February 1990 * the whole document *	1-13	
A	EP 0 675 532 A (PONT KABUSHIKI KAISHA DU ;NGK INSULATORS LTD (JP)) 4 October 1995 * the whole document *	1-13	
A	EP 0 654 818 A (CITIZEN WATCH CO LTD) 24 May 1995 * the whole document *	1-13	TECHNICAL FIELDS SEARCHED (Int.Cl.6) H05K H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
MUNICH	27 May 1997	Torti, C

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